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Group Art Unit: 2822

REMARKS

Restriction/Election

Applicant has elected claims 1-14, but respectfully submit for the record that the Restriction Requirement was with traverse and without waiving any rights for reconsideration of claims 15-20.

Claim Objections

Claim 7 was objected to because the term "bake" is misspelled in line 10. Applicant has amended claim 7 to replace "back" with "bake".

Claim Rejections - 35 USC §102

Claims 1-2 are rejected under 35 USC §102(b) as being anticipated by Long et al. (USPN 5,173,766, hereinafter "Long").

Applicant respectfully traverses the rejections since the Applicant's claimed combination, as exemplified in claim 1, includes the limitations not disclosed in Long of:

> "providing an oven having a wafer holder provided therein ;
> placing the semiconductor wafer on the wafer holder;
> applying mechanical pressure to the ILD layer on the semiconductor wafer...;
> and
> applying heat to the ILD layer on the semiconductor wafer...simultaneously with the applying the mechanical pressure." [deletions and underlining for clarity]

The above limitations relate to application of mechanical pressure and heat to an ILD (interlayer dielectric) layer on a semiconductor wafer in an oven. As well known to those having ordinary skill in the art, a semiconductor wafer includes a substrate with semiconductor devices covered by dielectric layers, which include one or more ILD layers.

The Examiner states in the Office Action, page 3, item 4:

> "Long et al. teaches placing a semiconductor wafer having an interlevel dielectric layer (ILD) on a wafer holder of an oven, applying mechanical pressure to the ILD layer using a mechanical device, and applying heat simultaneously with the mechanical pressure (Fig. 11, col. 14, lines 23-35, col. 32, lines 60-68, col. 33, lines 3-6). Long et al. shows applying the mechanical pressure includes relative motion to assist in planarization (col. 24, lines 7-20)."

However, Long discloses in the Long Abstract:

> "A semiconductor device package and a method of making such a package is described. The package comprises a flexible packaging substrate having a patterned metal layer...and a patterned insulative layer... A glob of silicone gel is deposited and cured on the *die*. A casting frame is connected to the metal layer...on the same side as the *die*. ... A...molding compound is then poured into the casting frame to define a moisture resistant package body."[underlining, deletions, and italics for clarity]

Thus, Long discloses a semiconductor device package and, as would be obvious to those having ordinary skill in the art, discloses processing after a semiconductor wafer is diced into separate die and sealed inside separate packages having a different substrate than the wafer substrate. Long does not disclose subject matter related to processing ILD layers.

The above is confirmed in Long Fig. 11, which shows the package substrate 30/34, and in Long col. 14, lines 23-35, which discloses:

> "The resulting sandwich 15 of top insulative layer 12, intermediate adhesive layer 10 and bottom metal layer 13a...is generically referred to...as a "three layer tape". Three layer tape 15 is...held on a planarizing surface...[T]he present invention utilizes a semi-rigid strip carrier...to bias the tape into a substantially planar form, but that the tape 15 retains its ability to flex out of its normal plane." [deletions and underlining for clarity]

Those having ordinary skill in the art would understand the "three layer tape" as the package substrate.

Also, Long col. 32, lines 60-68, states:

> "...the assembled compression fixture [for the package]...is placed in a curing oven...so that the backside and topside epoxies, 34 and 44, soften, flow together and simultaneously cure under the applied heat and pressure. The oven is set to a curing temperature approximately equal to or less than the maximum 160°C. glass transition temperature of the tape adhesive layer 10." [deletions and underlining for clarity]

Those having ordinary skill in the art would understand the assembled compression fixture as the fixture for the package substrate and not a semiconductor substrate. This would also be evident from the comment regarding the tape adhesive layer.

Further, Long col. 33, lines 3-6, states:

> "The compression fixture 1010/1040 is left in the oven for approximately 30 minutes. The recited temperature, time and pressure may be varied, of course, without interfering substantially with the adhesive flow and curing process."

Again, this clearly relates to a fixture for the package and not for an ILD layer.

Still further, Long col. 24, lines 7-20, states:

> "In each of the epoxy-dispense area 660 and die-attach area 670, a tape planarizing pedestal 610 is provided to reciprocate upwardly into contact with the bottom side of an overlying die-attach pad 14a. ...a uniform vacuum force can be applied to temporarily clamp the die-attach pad 14a flat against the planarizing surface 610 of the pedestal 610." [deletions and underlining for clarity]

Those having ordinary skill in the art would understand the tape planarizing to be an operation performed on a package substrate.

As stated in W.L. Gore & Assocs. v. Garlock, Inc., 721 F.2d 1540, 220 USPQ 303, 313 (Fed. Cir. 1983) (citing Soundscriber Corp. v. United States, 360 F.2d 954, 960, 148 USPQ 298, 301 (Ct. Cl.), *adopted*, 149 USPQ 640 (Ct. Cl. 1966)), *cert. denied*, 469 U.S. 851 (1984):

> "Anticipation requires the disclosure in a single prior art reference disclosure of each and every element of the claim under consideration."

It is respectfully submitted that claim 2 depends from claim 1 and contains all the limitations set forth in the independent claim 1 from which it depends.

Based on the above, it is further respectfully submitted that claims 1-2 are not anticipated under 35 USC §102(b) based on Long.

Claims 1-6 are rejected 35 USC §102(e) as being anticipated by Levert et al. (USPN 6,407,006, hereinafter "Levert").

Applicant respectfully traverses the rejections since the Applicant's claimed combination, as exemplified in claim 1, includes the limitations not disclosed in Levert of:

> "applying mechanical pressure...using a mechanical device; and
> applying heat...using the mechanical device simultaneously with the applying the mechanical pressure." [deletions and underlining for clarity]

The above claims applying heat using the mechanical device which is applying the mechanical pressure.

The Examiner in the Office Action pages 3-4, item 5, states:

> "Levert et al. teaches placing a semiconductor wafer having an interlevel dielectric layer (ILD) on a wafer holder of an oven, applying

mechanical pressure to the ILD layer using a mechanical device, applying heat simultaneously with the mechanical pressure (col. 7, lines 60-68, col. 26, lines 24-26). Levert et al. shows applying the mechanical pressure includes relative motion to assist in planarization, providing a non-sticking motion, sensing and controlling the temperature of the mechanical device (Abstract, col, 8, lines 5-15). Levert et al. shows the mechanical device using a roller (col 7, lines 20-27)."

However, Livert col. 7, lines 60-68, states:

"The dielectric precursor is applied to a surface to be planarized by any art-known method, e.g., including, but not limited to, spin-coating, dip coating, brushing, rolling, spraying and/or by chemical vapor deposition."

Claims 1-6 do not claim the application of the dielectric material and the above does not disclose the claimed subject matter,

Also, Livert col. 26, lines 24-26, states:

"Optionally, the film can be heated and cured while still under pressure in the press or after removal from the press."

This discloses that the dielectric film can be optionally heated and cured while under pressure but does not disclose how the heat is applied.

Further, the Livert Abstract, states:

"An apparatus for planarizing or patterning a dielectric film on a substrate is provided. The apparatus includes a press for applying contact pressure to an operably connected compression tool. The compression tool has a working face that is planar or patterned. A controller for regulating the position, timing and force applied by the compression tool to the dielectric film is also provided. There is also provided a support, with an optional workpiece holder for supporting the substrate and dielectric film during contact with the compression tool. Methods of using the apparatus, as well as planarized and/or patterned dielectric films are also provided."

The above does not disclose the application of heat since Livert considered this application of heat as being optional.

Still further, Livert col, 8, lines 5-15, states:

"Preferably, the contact surface of the object is fabricated or coated with a non-stick release material, e.g., Teflon.TM. or its functional equivalent. This can be in the form of a removable film or sheet of release material. Alternatively, the release material can be provided as a release coating directly on the compression tool working surface. The release material or coating can include any art-known materials, e.g., fluorocarbons, hydrocarbons, or other organic and/or inorganic materials which are either liquid or solid."

Claims 1-6 do not claim the material of the contact surface of the mechanical device and the above does not disclose the claimed subject matter. However, claims 21 and 22 have been added depending from claim 1 related to similar subject matter. The support for the claims is in Specification page 3, lines 21-23:

> "The thermally conducting non-stick surface 28 may be made to be consumed during the planarization of the low dielectric contant (low-k) ILD layer planarization to reduce friction and improve the surface characteristics of the ILD layer."

Continuing, Livert col 7, lines 20-27, states:

> Thus, for planariation (sic) objects having curved surfaces, it will be appreciated that contact between such a curved surface and the surface to be treated will be achieved with a rolling motion or rotating motion. In addition, it will be understood that the planarization object is typically incorporated into any art-known press or roller device to provide the mechanical force necessary to conduct the compression step according to the invention.

The above does not disclose or suggest the claimed limitation of applying heat using the mechanical device which is applying the mechanical pressure in an oven.

Claims 2-6 depend from claim 1 and contain all the limitations set forth in the independent claim 1 from which they depend.

Based on the above, it is respectfully submitted that claims 1-6 are not anticipated under 35 USC §102(b) based on Long.

Claim Rejections - 35 USC §103

Claims 7-14 are rejected under 35 USC §103(a) as being unpatentable over Levert in view of Oaks et al. (USPN 6,083,661, hereinafter "Oaks").

The Examiner states in the Office Action

> "Levert et al. teaches placing a semiconductor wafer having an interlevel dielectric layer (ILD) on a wafer holder of an oven, applying mechanical pressure to the ILD layer using a mechanical device, applying heat simultaneously with the mechanical pressure (col. 7, lines 60-68, col. 26, lines 24-26). Levert et al. shows applying the mechanical pressure includes relative motion to assist in planarization, providing a non-sticking motion, sensing and controlling the temperature of the mechanical device (Abstract, col. 8, lines 5-15). In addition, Levert et al. teaches spinning a low dielectric constant ILD material and curing the low dielectric constant ILD material (col. 3, lines 10-15, 53-60, col. 7, lines 45-65, col. 17, lines 17-55). Levert et al. shows the mechanical device using a roller (col. 7, lines 20-27)."

Furthermore, Levert et al. teaches an annealing process (col. 24, lines 53-60)."

Applicant respectfully traverses the rejections and the above statements since the Applicant's claimed combination, as exemplified in claim 1, includes at least one limitation not disclosed in Levert as explained above. Claim 7 includes the same limitation as claim 1 so the same reasons are incorporated here by reference thereto. It is also respectfully submitted that Oaks also does not teach or suggest this limitation.

The Examiner further states

"Levert et al. does not specifically describe soft baking the low dielectric constant ILD material at a soft bake temperature, holding the low dielectric constant ILD material at a temperature below the hard bake temperature (between 100°C. and 400°C.). However, Oaks et al. describes soft baking the low dielectric constant ILD material at a soft bake temperature, holding the low dielectric constant ILD material at a temperature below the hard bake temperature (between 100°C and 400°C), and hard baking the low dielectric constant ILD material (col. 16, lines 60-65, col. 17, lines 10-15, col. 19, lines 65-67)."

However, Oaks states in col. 16, lines 60-65:

"For a soft cured film on which additional metal or polymer layers will be formed, one may heat at 210°C. for 40 minutes.

For a hard or finally cured film, one may heat according to the following schedule:

50°C. for 5 minutes"

Further, Oaks states col. 17, lines 10-15:

"One may also cure the resin film in an infrared belt furnace. A suitable furnace and procedure are disclosed in P. E. Garrou et al., Rapid Thermal Cure of BCB Dielectrics, Proceedings ECTC, San Diego, May 1992, pp. 770-776. A Radiant Technology Corporation Model No. LA-306 infrared belt oven may be used with a nitrogen atmosphere. A soft cure may be obtained with a 1.5 minute residence at 260°C. A hard cure may be obtained with a 30 second residence at 280°C."

Still further, Oaks states in col. 19, lines 65-67:

"Residual solvent not removed during the spin-coating process is removed using a softbake cycle in an oven containing a nitrogen atmosphere at 80°C. for 0.5 hours."

It is respectfully submitted that none of the above teaches or suggests a combination of Oaks with Lavert. Also, there is nothing in Lavert that teaches or suggests a combination with Oaks.

The Court of Appeals for the Federal Circuit has held that a showing of a suggestion, teaching, or motivation to combine prior art references is an essential component of an obviousness holding. The Court emphasized that this need for specificity pervades precedential authority and reinforced the requirement that teachings of references can be combined only if there is some suggestion or incentive to do so (*In re* Fine, 837 F.2d 1071, 1075, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988)).

It is also respectfully submitted that the requirement for a prima facie case of obviousness under 35 USC §103 is that there must be:

> "...some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references." (*In re* Fritch, 972 F.2d 1260, 23 USPQ 2d 1780, 1783 Fed. Cir. 1992). [underlines added]

In re Dance, 160 F.3d 1339, 1343, 48 USPQ2d 1635, 1637 (Fed. Cir. 1998), followed and states there must be some motivation, suggestion, or teaching of the desirability of making the specific combination that was made by the applicant.

It is respectfully submitted that claims 8-14 depend from claim 7 and contain all the limitations set forth in the independent claim 1 from which they depend.

Claims 23 and 24 have been added depending from claim 7 related to the surface material of the mechanical device. The support for the claims is in Specification page 3, lines 21-23.

Based on the above, it is respectfully submitted that claims 7-14 and 23-24 are unobvious under 35 USC §103(a) based on Levert in view of Oaks.

The other references cited by the Examiner showing the prior art have been considered and are not believed to disclose, teach, or suggest, either singularly or in combination, Applicant's invention as claimed.

Conclusion

In view of the above, it is submitted that the claims are in condition for allowance and reconsideration of the rejections is respectfully requested. Allowance of claims 1-14 and 21-24 at an early date is solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby mad . Please charge any shortag in fees due in connection with the filing of this

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paper, including any extension of time fees, to Deposit Account No. 50-0374 and please credit any excess fees to such deposit account.

Respectfully submitted,

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NOTE: The "VERSION WITH MARKINGS TO SHOW CHANGES MADE" begins on the following page.

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

- Please amend claim 7 by inserting the underlined text and deleting strike-through text as follows:

7. (Amended) A method for planarization of low dielectric constant ILD layers on a semiconductor wafer comprising:

providing an oven having a rotatable wafer holder provided therein ;

placing the semiconductor wafer on the wafer holder;

rotating the wafer holder with the semiconductor wafer thereon;

spining on the low dielectric constant ILD material on to the semiconductor wafer in the oven;

soft baking the low dielectric contstant ILD material at a soft bake temperature in the oven;

holding the low dielectric constant ILD material at a temperature below the hard ~~back~~ bake temperature in the oven;

applying mechanical pressure to the ILD layer on the semiconductor wafer using a mechanical device to apply rotating pressure to the ILD layer in the oven;

applying heat to the ILD layer on the semiconductor wafer through the mechanical device simultaneously with the applying the mechanical pressure in the oven;

hard baking the low dielectric constant ILD material at a hard bake temperature in the oven;

cooling the low dielectric constant ILD material in the oven; and

annealing the low dielectric constant ILD material in the oven.